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Design and Analysis of Nanotube-Based Memory Cells

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Abstract In this paper, we proposed a nanoelectromechanical design as memory cells. A simple design contains a double-walled nanotube-based oscillator. Atomistic materials are deposed on the outer nanotube as electrodes. Once the WRITE voltages are applied on electrodes, the induced electromagnetic force can overcome the interlayer friction between the inner and outer tubes so that the oscillator can provide stable oscillations. The READ voltages are employed to indicate logic 0/1 states based on the position of the inner tube. A new continuum modeling is developed in this paper to analyze large models of the proposed nanoelectromechanical design. Our simulations demonstrate the mechanisms of the proposed design as both static and dynamic random memory cells.

Keywords Carbon nanotube · Memory cells · Continuum model

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Introduction

Due to their unique mechanical and electronic properties [1, 2], carbon nanotubes hold promise in designing novel nanoscale devices, such as scanning probe tips, field emission sources, molecular wires, and diodes. For example, Bachtold et al. [3] designed logic circuits with field-effect transistors using individual carbon nanotubes (CNT). Kinaret et al. [4] investigated the operational characteristics of a nanorelay in which a conducting CNT was placed on a terrace in a silicon substrate. Other proposed CNT-based devices include nanotube resonant oscillators [5], nano cantilevers [6], nanotube motors [7], and others. One of the exciting designs, proposed by Rueckes et al. [8], was nanotube-based non-volatile random access memory. In this design, each device element was based on a suspended, crossed nanotube geometry that leads to bistable, electrostatically switchable on/off states. Due to small size and low interlayer friction [9], double-walled nanotubes (DWNT) have been utilized as co-axial oscillators [10–12], which can have oscillation frequencies up to 72 GHz [13]. Based on our previous investigations [13], we propose a conceptual design of nanotube-based memory cells in this paper and study the mechanisms of this device as static random access memory (SRAM) and dynamic random access memory (DRAM).

Molecular dynamics simulations [13] have shown that nanotube-based co-axial oscillators could cease at finite temperatures due to the interlayer friction between the inner and outer tubes. A higher temperature results in faster energy dissipation because of the larger interlayer friction. Consequently, stable oscillations could not be observed. To overcome the above issue, we propose a nanoelectromechanical (NEMS) design containing a nanotube-based co-axial oscillator to provide stable oscillation so that this

design can be employed as memory cells. We also develop a continuum model in this paper to analyze the proposed NEMS memory cell design.

Design of Memory Cells

Figure 1 illustrates a simple example of the proposed NEMS design. The outer tube is a capped (17, 0) zigzag tube while the inner tube is a capped (5, 5) armchair tube. It has been known that CNTs with different chiralities exhibit different electrical properties. Generally, a pair of integers (m, n) is employed to represent the chirality of a nanotube. If $(m - n)/3$ is an integer, the CNT is metallic; otherwise, the tube is semiconducting. In the proposed design, the outer tube is semiconducting while the inner tube can be either metallic or semiconducting. For instance, a (17, 0) nanotube is semiconducting while a (5, 5) nanotube is metallic. In the example depicted in Fig. 1, the outer tube is positioned on the top of a conducting ground plane. The ground plane would be a (100) gold surface which would be thick enough to achieve low conductivity over the entire ground plane—probably less than 10 monolayers would be sufficient. In this paper, we have not considered the interaction between the ground plane and the nanotube. However, deflection due to such interaction would tend to reduce the dynamics of the inner nanotube, leading to some additional damping. Consequently, the device is easier to control with slightly less frequency response. According to the stiffness and small diameter of the nanotubes investigated here, such an effect would be minimal.

Atomic materials for the conducting electrodes 1 and 2 are deposited on the top of the outer nanotube. The electrode composition would be gold as well. Evaporation is certainly one mechanism for deposition of the electrode. It may also be possible to deposit the electrode by molecular beam epitaxy techniques. Using such techniques, the gold atoms will tend to bond with the carbon atoms at the outside surface of the nanotube, preventing their deposition on the inside of the nanotube.

In this configuration, the inner tube sits in a double-bottom electromagnetic potential well. The depth of the potential well under electrode 1 is proportional to the voltage applied to electrode 1; similarly, the depth of the potential well under electrode 2 is proportional to the voltage applied to electrode 2. The induced quasi-static electromagnetic forces exerted on the inner tube will overcome interlayer friction if the applied voltage is sufficiently large. This large applied voltage is referred to as the WRITE voltage. When a WRITE voltage is applied to the electrode, the inner tube may move due to the induced electromagnetic forces [14, 15]. Consequently, lateral motion of the inner tube will be induced as a result. Here, a capped outer tube is employed because the inner tube can easily escape from an open outer tube due to the induced electromagnetic forces. The capacitance of the NEMS gate can be read by a distinct READ process. A constant-current pulse is applied to one of the electrodes. If the inner CNT is present under that electrode, a relatively large capacitance will be observed, and the time required to charge the electrode will be longer. If the inner tube is not present under that electrode, a relatively small capacitance will be observed, as will a concomitant fast charging time for the electrode. As a result, the logic state of the NEMS gate can be determined. It should be noted that all READ voltages are sufficiently small so that the motion of the inner tube will not be influenced. Less than 5% of the WRITE voltage is recommended for the READ voltage. Whether the inner tube is underneath electrode 1 or electrode 2 will result in two different physical states determined by the READ voltage. These two different physical states can be interpreted as Boolean logic states. Therefore, the system can be used as a random access memory (RAM) cell. It should be noted that Kang and Hwang [16] proposed the similar NEMS design, called 'Carbon nanotube shuttle' memory device. However, our design is more specific, and we quantitatively illustrate the proposed design as SRAM and DRAM cells. In addition, the continuum model developed in this paper will help to study feasibility of large nanotube-based memory cells in practical applications.

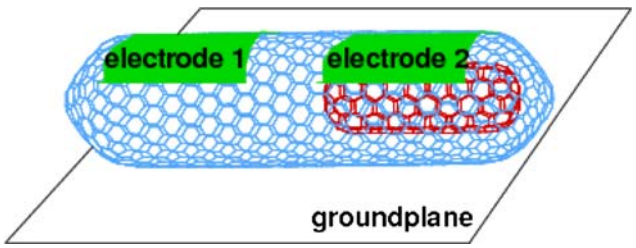

Fig. 1 A NEMS design for memory cells

Fabrication of arrays of nanotube structures such as we propose in this paper is a subject of much ongoing research. CNT geometric uniformity and the ability to position CNTs in a regular array suitable for addressing as a RAM memory cell are both issues that remain open. However, significant progress in this area is being made. In previous research [17], the researchers reported on a complete scheme for creating predefined networks of individual CNTs. Using a specialized CVD method to grow single-walled carbon nanotubes (SWNTs) on SiO2-capped Si pillars, coupled with spectroscopic techniques to map the specific tube geometries, the fabrication of regular arrays of CNTs suitable for use in integrated circuits has been demonstrated. Extension of these or other techniques for fabricating regular arrays of DWNTs will be required to implement our memory cell beyond the proof-of-concept stage.

Continuum Modeling

Carbon nanotubes observed in experiments [18] always contain more than millions of atoms. Consequently, MD has difficulties in studying the feasibility of the proposed NEMS design in practical applications. In this paper, we employ a continuum approach, the mesh-free particle method [19], to model the memory cell via discretizing the shells of nanotubes as particles. During the simulation, the outer tube is fixed and has no deformation. We first assume that the inner tube is deformable. Therefore, the following equations of motion are solved at each particle on the inner tube:

$$m_{\mathrm{I}}\mathbf{u}_{\mathrm{I}} = \mathbf{f}_{\mathrm{I}}^{\mathrm{ext}} - \mathbf{f}_{\mathrm{I}}^{\mathrm{int}} \tag{1}$$

where m_{I} is the mass associated with particle I, $\mathbf{u}_{\mathrm{I}}$ is the displacement of particle I, and $\mathbf{f}_{\mathrm{I}}^{\mathrm{int}}$ is the internal nodal force applied on particle I due to the deformation of the nanotube itself. The external nodal force, $\mathbf{f}_{\mathrm{I}}^{\mathrm{ext}}$, contains two parts. One is due to the interlayer interaction between the inner tube and the outer tube, and the other is the induced electromagnetic force when applying voltage on the electrodes.

Generally, the Lennard-Jones 6–12 potential [12] has been employed to describe the van der Waals interaction between shells in a multi-walled carbon nanotube (MWNT) in a molecular model. The potential function is written as

$$\phi(r) = A\left[\frac{1}{2}\frac{y_0^6}{r^{12}} - \frac{1}{r^6}\right] \tag{2}$$

where $A = 2.43 \times 10^{-24}$ J nm and $y_0 = 0.3834$ nm. The interlayer equilibrium distance is 0.34 nm, which results in the minimum van der Waals energy. This distance matches the thickness of a graphene sheet, and it also satisfies the criterion proposed by Legoas et al. [11] for stable nanotube-based oscillators.

In the mesh-free particle model, the major issue is how to calculate interaction between particles at different layers in an MWNT to approximate molecular-level interlayer interaction. To solve this issue, we choose two representative cells of area S_0, each containing n nuclei ($n = 2$ in this paper for graphene sheets). The continuum-level van der Waals energy density is defined as

$$\varphi(d) = \left(\frac{n}{S_0}\right)^2 \phi(d) \tag{3}$$

where $d = \|\mathbf{x}_{\mathrm{O}} - \mathbf{x}_{\mathrm{I}}\|$ is the distance between the centers of those two considered cells. One is on the outer tube, and the other is on the inner tube. Then, the total continuum-level non-bonded energy is calculated as

$$\Phi = \int_{\Omega_{\mathrm{O}}}\int_{\Omega_{\mathrm{I}}} \varphi(\|\mathbf{x}_{\mathrm{O}} - \mathbf{x}_{\mathrm{I}}\|)\mathrm{d}\Omega_{\mathrm{I}}\mathrm{d}\Omega_{\mathrm{O}} \tag{4}$$

where Ω_{O} and Ω_{I} are the configurations of the outer and inner tubes, respectively. Then, the force applied on particle I can be derived as the first derivative of Φ with respect to the coordinates of particle I.

It should be noted that Φ is the interlayer potential when atoms are placed at the equilibrium positions. Therefore, interlayer friction due to atoms' thermal vibration cannot be directly calculated from the continuum approximation. We employ MD to simulate nanotube-based oscillators at the room temperature of 300 K. The interlayer friction, which causes the energy dissipation, is calculated as 0.025 pN per atom. In all, the external force applied due to the interlayer interaction is

$$\mathbf{f}_{\mathrm{I}}^{\mathrm{ext1}} = \frac{\partial\Phi}{\partial\mathbf{x}_{\mathrm{I}}} - 0.025N\frac{v_{\mathrm{I}z}}{|v_{\mathrm{I}z}|}\mathbf{e}_z \tag{5}$$

where $v_{\mathrm{I}z}$ is the z component of the velocity of particle I, and N is the number of atoms represented by particle I in the mesh-free particle model. Here, $\mathbf{e}_z$ represents direction along the nanotube axis.

In the proposed NEMS design, an electrode of potential V with the ground plane that has the zero potential can be viewed as a capacitor. Its capacitance is expressed as

$$C = \frac{\int_S \mathbf{E}\cdot\varepsilon_0\mathrm{d}\mathbf{S}}{V} \tag{6}$$

where $\boldsymbol{E}$ is the electric field and $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m is the permittivity of free space (in farads per meter). Since the energy stored in a capacitor is $W = \frac{1}{2}CV^2$, the induced electrostatic force can be calculated as

$$\mathbf{f}_{\mathrm{I}}^{\mathrm{ext2}} = \left.\frac{\partial W}{\partial z_{\mathrm{I}}}\right|_V \mathbf{e}_z = \frac{1}{2}V^2\frac{\partial C}{\partial z_{\mathrm{I}}}\mathbf{e}_z \tag{7}$$

where z_{I} is the axial position of the atom on the inner tube. The electromagnetic forces are in the direction of the higher electric field density and therefore serve to localize the inner nanotube underneath the electrode with the higher applied WRITE voltage. We only consider the axial electrostatic forces because: (1) the motion of the inner tube is along the axial direction, and (2) the transverse electromagnetic forces are small enough to be ignored. The classical conductor model is used here to approximate the electrostatic field induced in the proposed NEMS design. Consequently, equations of motion, i.e., Eq. 1, can be rewritten as

$$m_{\mathrm{I}}\mathbf{u}_{\mathrm{I}} = \frac{\partial\Phi}{\partial\mathbf{x}_{\mathrm{I}}} - 0.025N\frac{v_{\mathrm{I}z}}{|v_{\mathrm{I}z}|}\mathbf{e}_z + \frac{1}{2}V^2\frac{\partial C}{\partial z_{\mathrm{I}}}\mathbf{e}_z - \mathbf{f}_{\mathrm{I}}^{\mathrm{int}}. \tag{8}$$

Results and Discussions

We first analyze mechanisms of the proposed NEMS design as SRAMs. A (17,0)/(5,5) DWNT is employed in the memory cell. The length of the (17, 0) outer tube is 6.4 nm, while the length of the (5, 5) inner tube is 3.7 nm. Two 2.0-nm-long electrodes are deposed on the top of the outer tube symmetrically. A constant voltage of 16 V with a time interval of 1 ns is applied on those two electrodes alternatively. Initially, the inner tube is at the center of the outer tube, as shown in Fig. 2.

When the inner tube is under electrode 1 or electrode 2, its position can be detected by the READ process and the logic states 0 and 1 are produced. Figure 3 shows the position of the inner tube at different logic states. The red color on the electrode indicates that this electrode is applied a WRITE voltage. From the described mechanism, we found that the frequency of the memory cell depended on the frequency of the voltage shifting. In other words, the memory cell works as a SRAM. In this case, the frequency of this SRAM is 500 MHz. The maximum available frequency for SRAM depends on the maximum frequency of the applied signals. It should be possible to achieve

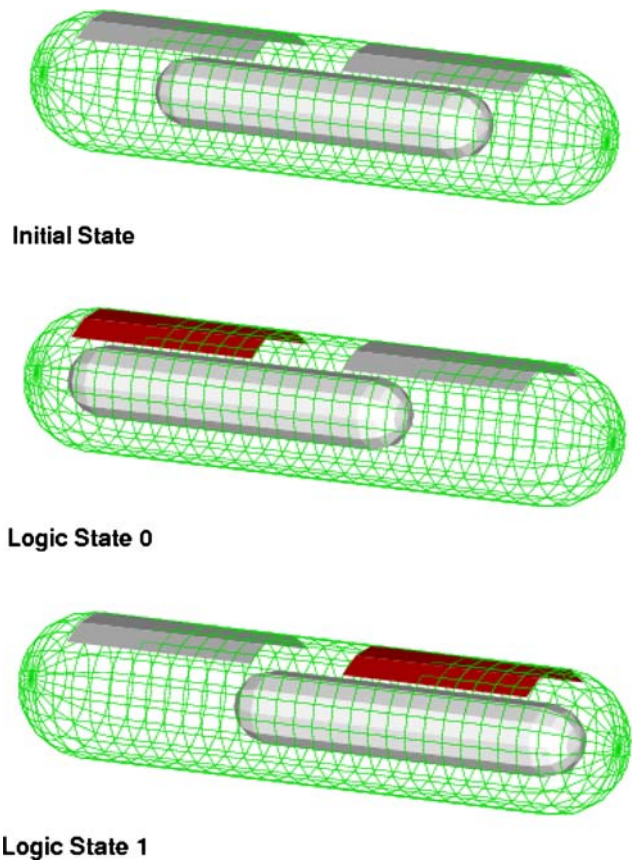

Fig. 2 Positions of the inner tube at different logic states in SRAM configuration

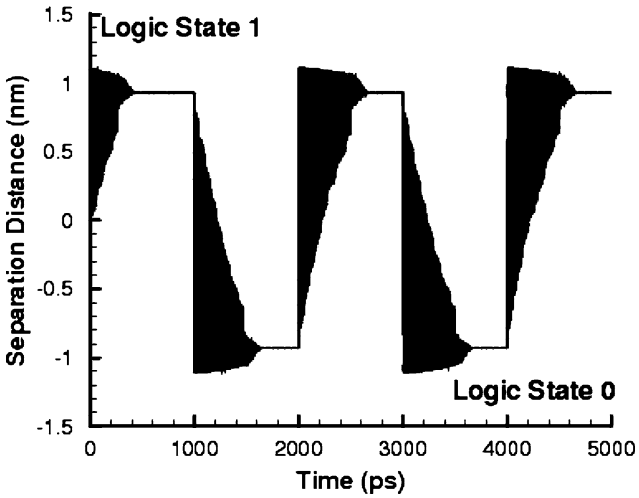

Fig. 3 Separation distance of the short nanotube-based memory cell in SRAM configuration

frequencies of 10–100 GHz with current device technology. The SRAM device would be useful at the lower end of this frequency range.

It is obvious that the frequency of the SRAM cell cannot exceed the natural frequency of its embedded nanotube-based oscillator. Since the nanotube-based oscillator is an underdamped system, the proposed design can be extended for application as a DRAM cell. In this configuration, the oscillator will continue to oscillate at its natural frequency. A WRITE voltage pulse is applied every several oscillation periods to stimulate oscillation of the oscillator. Consequently, a steady oscillation can be generated for logic states 0 and 1. As an example, the simulated DRAM cell included a 32-nm-long (17, 0) outer tube and an 18-nm-long (5, 5) inner tube. The open-ended outer tube instead of the capped one is employed. In this case, two 10-nm-long electrodes are attached on the top of the outer tube. Initially, the inner tube has a velocity of 400 m/s and is placed at the center of the outer tube. In this case, the natural oscillating frequency of the oscillator is 6.75 GHz. After every four cycles, a voltage of 48 V with a duration of 2 ps is applied at the electrode to increase the oscillatory amplitude. Consequently, the inner tube keeps a stable oscillation.

Figure 4 illustrates the evolution of separation distance between the inner tube and the outer tube. It has demonstrated the mechanism of this memory cell as DRAM, which has a frequency of 6.75 GHz. In addition, Fig. 5 shows the configurations of this memory cell at different logic states. In Fig. 5, the outer tube is not shown except its ends as rings. It should be noted that although the WRITE voltages are applied on a single electrode, both electrodes are needed for applying READ voltages to detect logic states.

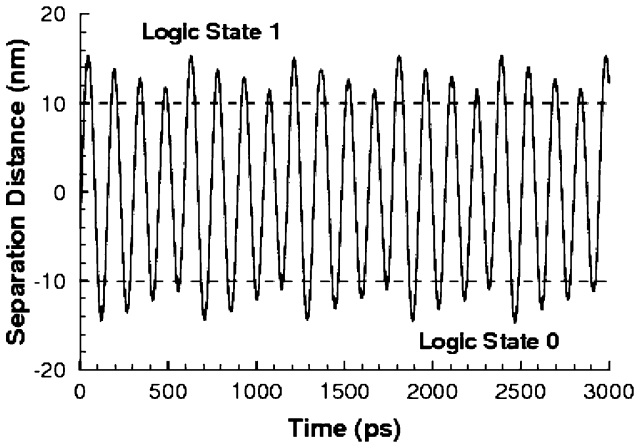

Fig. 4 Separation distance of the long nanotube-based memory cell as DRAM

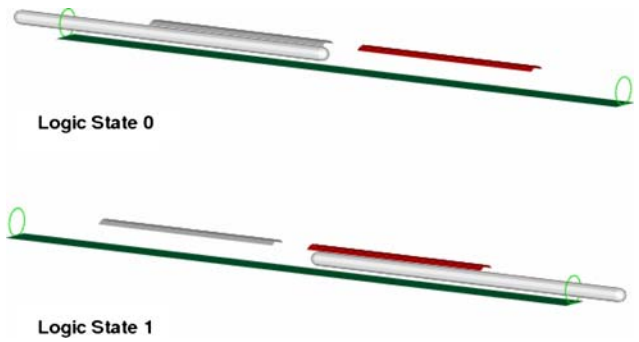

Fig. 5 Configurations of DRAM in different logic states

Nanotube-based oscillators can provide high oscillation frequencies. However, it is found that the oscillation could cease due to interlayer friction between the inner and outer tubes when the oscillator is at finite temperatures. Such a shortcoming prevents the nanotube-based oscillators from being utilized in nanodevices. We designed a new NEMS device via deposing atomic materials on the top of the outer tube as electrodes. Once a voltage is applied on the electrodes, the induced electrostatic force can overcome the interlayer friction. We developed a multiscale method to simulate the proposed design. Our simulations demonstrated that the designed device can be utilized as SRAM and DRAM. In this paper, the design and analysis procedure can be extended for other NEMS designs.

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