

A VERILOG HDL DIGITAL ARCHITECTURE FOR DELAY CALCULATION

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Abstract— A method for the calculation of the delay between two digital signals with central frequencies in the range [20, 300] Hz is presented. The method performs a delay calculation in order to determine the bearing angle of a sound source. Computing accuracy is tested against a previous implementation of the Cross Correlation Derivative method. A Verilog RTL model of the method has been tested on a Xilinx® FPGA in order to evaluate the real performance of the method. Simulations of an ASIC design on a standard CMOS technology predict a power saving of about 25 times per delay stage over previous implementations.

Keywords— Verilog, FPGA, low power, digital CMOS VLSI.

I. INTRODUCTION

Methods for the detection of sound sources have been widely studied, including the use of complex techniques such as Independent Component Analysis, Cross-correlation analysis (Carter, 1987; Knapp and Carter, 1976; Riddle, 2004), Gradient Flow techniques (Stanacevic and Cauwenberghs (2005), and the emulation of the human hearing cochlea (Shamma *et al.*, 1986; Lazzaro and Mead, 1989; Horiuchi, 1995), some of which have been successfully implemented in analog and digital VLSI circuits (Lazzaro and Mead, 1989; Horiuchi, 1995; Harris *et al.*, 1999; Grech *et al.*, 1999; van Schaik and Shamma, 2004). There are only a few cases in the literature where low power integrated circuits have been implemented for this task. Van Schaik and Shamma (2004) implemented an integrated circuit (IC) based on an analog cochlea using a 0.5 μ m process in an area of 5 mm². In this case, the power dissipation depends strongly on the input signals. With no activity, the cochlear channels dissipate 400 μ W; for a time delay of 100 μ s (corresponding to a 77° angle incoming signal), the power dissipated is 1.85 mW. Stanacevic and Cauwenberghs (2005) implemented a 3 mm by 3 mm, 0.5 μ m CMOS technology IC with a method based on analog processing at a sampling rate of 16 kHz, which discriminates 2 μ s with a power consumption of 32 μ W. A third implementation, proposed in Julián *et al.* (2004) and successfully implemented in Julián *et al.* (2006), is based on a cross-correlation derivative algorithm. This

method features an accuracy of one degree for angles in the range = [0,50] U [+130,+180] for signals between [20 Hz, 200 Hz], using two detectors (i.e. four microphones) to cover the whole 360 degrees without accuracy loss. The integrated circuit (IC) designed by Julián *et al.* (2006), allows for this with less than 600 μ W of power dissipation (for a full quadrant bearing estimation) on a 0.35 μ m technology with measures of 2 mm by 2.4 mm.

An alternative method for the estimation of such angle is proposed in this paper in order to reduce power dissipation still further, while keeping calculation performance. The problem is to determine the direction of a sound source picked by an array of microphones such as the one in Fig. 1. The digital signals are provided from this array after being conveniently conditioned. The cross-correlation derivative (CCD) approach is a variation of the standard time-domain cross-correlation between two signals. The CCD algorithm works with a one bit discrete quantization of the input signals, and therefore, reduces drastically the complexity of the resulting digital circuitry. Another feature is that the spatial derivative of the cross-correlation is calculated instead of the cross-correlation itself. Calculation of the CCD results in an activity reduction of a thousand times in the digital circuitry. In the case of the standard cross-correlation approach, once the partial correlations are calculated, the maximum needs to be evaluated which requires a dedicated stage. In the CCD, it is only necessary to locate a change in the output value of the partial correlations (which are either 1 or 0), making this task trivial: one only needs to detect transitions of the input signals.

The strategy proposed in this paper is to use a single counter for delay measurement together with an adaptive closed loop system. The closed loop guarantees stability, and also a convergence of the counter count to the delay under measurement. The reduction of power consumption is a consequence of the reduction in size of the circuitry. In fact, just one counter is needed as opposed to the 104 10-bit counters used in the implementation proposed by Julián *et al.* (2006).

The paper is organized as follows. Section II describes the Verilog HDL front-end implementation of the proposed structure for the detection of transitions

and the calculation of the respective delay. Section III analyses simulations and test runs on a Xilinx® Spartan3 FPGA to provide data for contrast against previous results obtained by Julián *et al.* (2006). Section IV shows comparisons of functional and power performance between the implementation in Julián *et al.* (2006) and the simulation results of a 0.5 μm ASIC design of the proposed architecture.

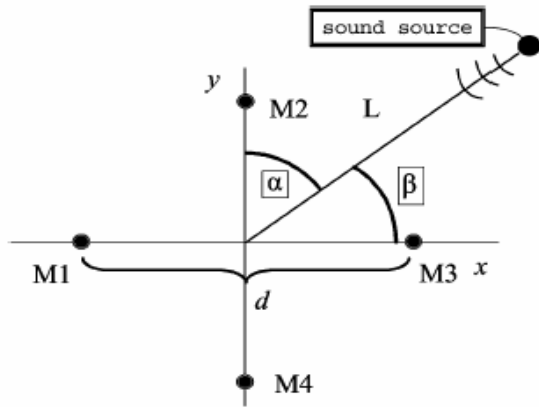


Fig. 1. Microphone array to measure the bearing angle from a sound source

II. STRUCTURAL DESIGN (FRONT-END)

A. Basic Structure

The first objective is to obtain, at least, the same accuracy as in the previous implementation by Julián *et al.* (2004). Any degrading in the method’s accuracy would render useless any further improvements in the rest of the circuit’s features. The front-end design was coded using Verilog HDL and the Xilinx® Integrated Software Environment (ISE) and implemented on a Spartan3 Digilent Inc. prototyping board. Simulations were run on Mentor Graphics® ModelSim® HDL simulator. Figure 2 depicts the basic structure, composed of a block that captures and stores the signals being measured, and a second block which calculates the delay. The output has a tri-state control (*oe_L*) to allow its interfacing to a general data bus, with two extra signals providing information about the state of the unit, i.e., if it is out of its measurement range (*out_range*) and if data is available (*data_rdy*).

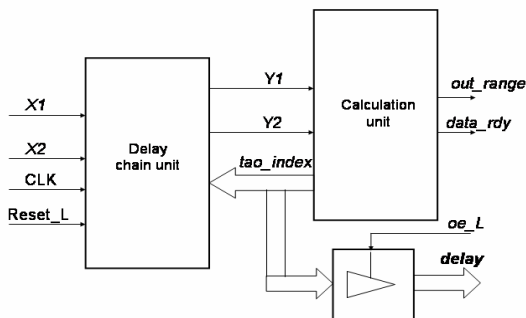


Fig. 2. Block diagram of front-end design

A frequency divider was implemented for the generation of the 200 kHz clock from the board’s 50MHz oscillator. Xilinx® Digital Clock Managers were not used in order to avoid technology dependent code. Nonetheless, global clock buffers were instantiated using Xilinx® Verilog primitives’ libraries, thus protecting generated clock signals from excessive fan out. These extra buffers can be easily removed if another programmable technology is to be used, or if the code is to be synthesized for a particular MOS technology.

B. Delay Chains

The first block, shown in Fig. 3, captures the signals at a 200 kHz rate. This rate has been chosen in order to attain an estimation accuracy of one degree for angles in the range = [0, 50] U [+130, +180] for signals between [20Hz, 200 Hz], as stated in Julián *et al.* (2004). Data is stored in two Serial In-Parallel Out registers that serve as delay chains. Considering such speeds, the circuit proposed would allow for the measurements of ±620 μs of delay, increasing thus the range of the system implemented by Julián *et al.* (2006).

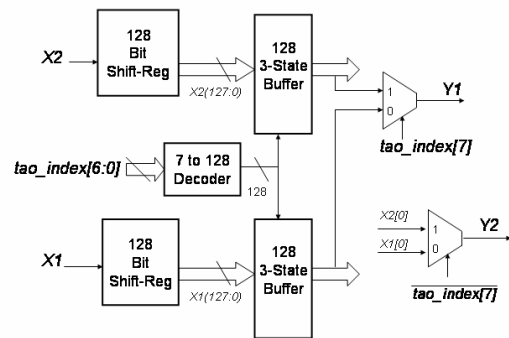


Fig. 3 Block diagram of the delay chain

Registers and multiplexers are generated using Verilog’s generic parameters so as to speed up post placement simulation times (one can instantiate shorter multiplexers and registers before a particular simulation that does not use the whole structure, and then return to their full size version for a test on the FPGA, all with a simple parameter overloading on the parent modules and a recompilation of the ISE’s project).

For reference’s sake, it is always assumed that signal X1 leads X2. The first bit of one of the chains (by convention X2) is used as base pointer, while the other chain is swept in search of transitions by the signal *tao_index*. This index is an 8-bit signed integer in two’s complement. The sign bit switches the multiplexers in the case where X1 is actually lagging X2, instead of leading. Thus, the base pointer is switched to X1[0] and the index’s magnitude is used to sweep X2. In order to do this using just one decoder, X2’s selection signals are wired backwards (as it can be noticed in the code above). An error of minus one tap (minus 5μs at a sampling rate of 200 kHz) is introduced using this scheme,

because of the base being actually displaced minus one bit as a result of the switching. This error is considered negligible, and can be easily corrected by the software of the system receiving the final data.

Due to the shortage of tri-state buffers in the chosen FPGA (only available in the IO blocks), the synthesizer was allowed to substitute the big 128 tri-state buffers with pull-up logic. This will not be the case in an ASIC implementation.

C. Calculation Unit

The calculation unit in Fig. 4 must discover valid transitions in the input signal to account for an increase or decrease of the index counter, depending on the index sign bit. Repeated application of the calculation will produce a monotonic estimation of the target delay. Since the circuit is designed to increase or decrease its count by one on each valid transition, the convergence time is determined by:

$$T_{convergence} = \frac{1}{2} * \frac{1}{f_{signal}} * Signal\ delay * f_{CLK}, \quad (1)$$

In its worst case (maximum delay of 400 μ seg for a 200 Hz signal) this convergence time is still well within the proposed estimation period of one second. An *out_range* signal is provided to indicate the saturation of the index counter. This serves as an auxiliary signal to allow for the adaptive measurement of faster or slower signals via the modification of the clock speed.

For the validation of the transitions, the signals pass through two FFs (Fig. 4). The decision logic determines whether to increase, decrease or leave the counter unchanged depending on the arrival order of the transitions and *tao_index*'s current state. Transitions are checked on the rising and falling edges of the signals as seen in Fig. 5. Evaluation thus occurs at a speed twice as fast as the signal's frequency (on a noise-free signal). The decision logic is registered in order to eliminate the chance of falsely locking the circuit to the same transition. This avoids a run-up of the counter.

Table 1 shows a summary of the resources used in the Spartan3.

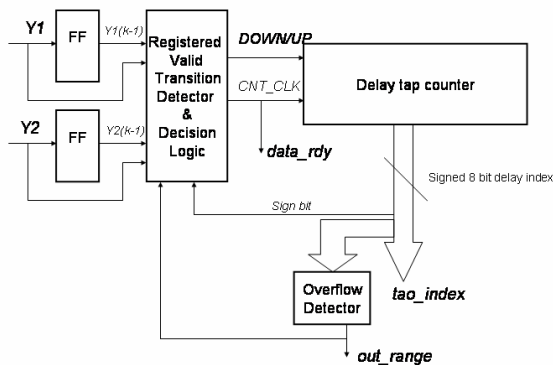


Fig. 4. Computing of the index for the delay chains (delay between X1 and X2)

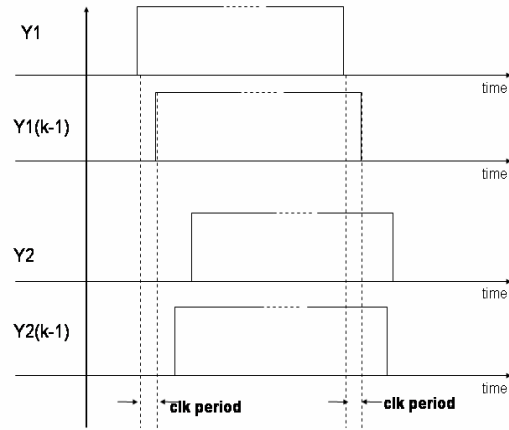


Fig. 5. Signals fed to the valid transition detector and counting decision logic. In this case, a transition en Y1 is detected while Y2 remains constant. Counter is increased if sign bit is 0 or decreased otherwise.

Table 1. Resources Used on Selected Device 3s200ft256-5, reported by Xilinx® ISE

Resource		Percentage
Number of Slices	194 out of 1920	10%
Number of Slice Flip Flops	267 out of 3840	6%
Number of 4 input LUTs	205 out of 3840	5%
Number of bonded IOBs	5 out of 173	2%
IOB Flip Flops:	3	
Number of GCLKs	2 out of 8	25%

III. FUNCTIONAL TESTING AND ANALYSIS OF FRONT END IMPLEMENTATION

A. Functional Simulation and FPGA Testing

Simulations were run at the RTL level and the gate level (with back annotation from the post placement and routing models written by ISE®). Results from the ModelSim® simulator were fed into Matlab® for a preliminary check of the accuracy of the method. A set of files with test signals was created in Matlab® to serve as stimulus signals to the simulator. In addition, simulations were also performed using real signals taken from previous experiments on the same system reported in Julián *et al.* (2006).

The final tests were executed on a Spartan 3 Digilent Inc. board, with the input signals fed from a programmable delay generator written in VHDL and implemented on another Spartan 3 board. The outputs were fed to the computer through a PMD-1608FS Measurement Computing® acquisition board.

The measured data was processed in Matlab® to produce an analysis of the signals. There was also a measurement of the convergence time when the output evolves from a steady state to another after a sudden change in the delay being measured. Figure 6 shows the case when the input delay is suddenly changed from 0 to 325 μ s (65 delay units at a sampling speed of 200 kHz). The convergence time in the graph is equal to the time predicted by (1).

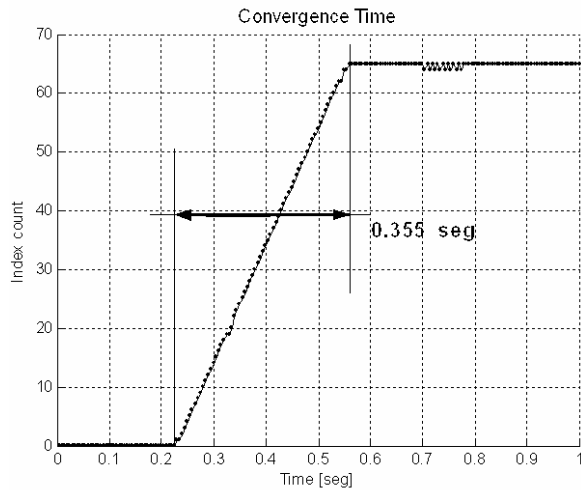


Fig. 6. System’s calculation transient of a sudden change in the input delay (0 to 325 μs).

B. Improvement of Decision Logic and Delay Calculation

Boolean equations for the control of the delay counter, DN_UP (2) and CNT_CLK (3) were obtained using Berkeley’s Espresso minimization algorithm and were tested on the FPGA by directly introducing them into the RTL code instead of the high level decision sentences used in the original front-end implementation.

$$DN_{UP} = \overline{SGN} * (A+B) + \overline{SGN} * \overline{OVN} * (C+D) \tag{2}$$

$$CLK_{CNT} = \overline{SGN} * \overline{OVP} * (C+D) + \overline{SNG} * \overline{OVN} * (C+D) + (A+B) \tag{3}$$

$$A+B = \overline{Y_1} * Y_{1_K1} * \overline{Y_2} * Y_{2_K1} + Y_1 * \overline{Y_{1_K1}} * Y_2 * Y_{2_K1} \tag{4}$$

$$C+D = \overline{Y_1} * Y_{1_K1} * Y_2 * Y_{2_K1} + Y_1 * \overline{Y_{1_K1}} * \overline{Y_2} * Y_{2_K1} \tag{5}$$

A similar performance was obtained with simulations executed on both the RTL and the Boolean generated code. Tests were also run on the FPGA, contrasting both sets of code using Matlab® for verification.

This part of the circuit is not as critical as the delay chains from the viewpoint of power dissipation because in the worst-case condition (maximum delay between X1 and X2), the counter operates at a maximum speed equal to twice the input signal frequency, which is a low frequency signal. However, efforts were made to keep logic and registers at a minimum.

IV. POWER AND PERFORMANCE CONSIDERATIONS

In order to compare the architecture’s performance in terms of accuracy and power dissipation, a design using a standard CMOS 0.5 μm technology was simulated. Due to the lack of standard cells specifically made for low power purposes, a schematic based on the logical Verilog design was drawn on Tanner® S-Edit, including all the constraints regarding power consumption. Based on this schematic, a layout of the circuit was drawn using Tanner® L-Edit, from which a SPICE model was extracted for its simulation on Mentor Graphics® Eldo and Mach-TA for analog timing checking, power estimations and digital verification.

A. Performance Comparison

As already seen, the Delay Chain unit must operate at 200 kHz and, considering its size and operation speed, it would be responsible for the maximum power dissipation on an IC designed with the proposed architecture. In order to minimize power consumption, the SIPO delay chains were built using C²MOS registers. This master-slave edged triggered register does not need feedback, as the data is stored in the internal node capacitances, and features a lower clock fan-in and a smaller area compared with the eighteen transistors required for a static register (Rabaey *et al.*, 2003).

Eldo Spice simulations were run with the whole unit of 256 registers connected plus the selection logic, all supplied with 3.3 V to obtain a preliminary estimation of the power dissipation. Results from simulations and average values calculated are shown in Fig 7 and Table 2, compared against data from previous implementations by Julián *et al.* (2006), Stanacevic and Cauwenberghs (2005), and Schaik and Shamma (2004). As it is shown, the power dissipation is significantly reduced with savings of 49.5, 2.66 and 154 times respectively. All this is achieved with a notable improvement of the system’s measurement range.

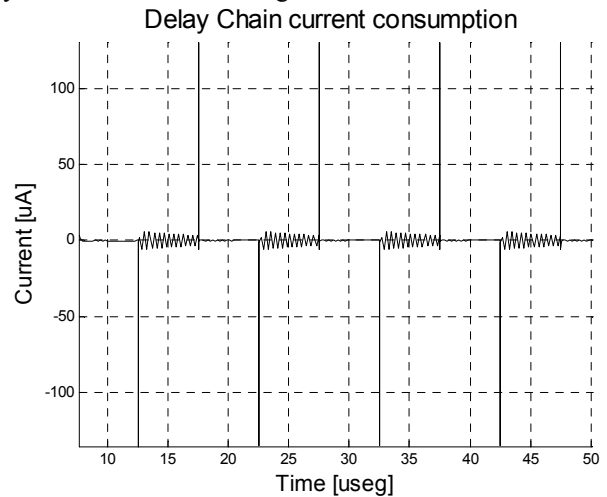


Fig. 7. Current drawn by a 256 C²MOS master-slave register delay chain.

Table 2. Comparison of total power consumption between systems

Unit	Total Unit Power (uW)	Tech. (μm)	Area	Power saving factor
Neuromorphic sound localizer (Schaik, 2004).	1850	0.50	5mm x 5mm	154
Micropower gradient flow (Stanacevic, 2005)	32	0.50μm	3mm x 3mm	2.66
Cross-correlator (Julián, 2006).	594	0.35μm	2mm x 2.4mm	49.5
Adaptive (from Mentor Graphics® Eldo Spice)	12	0.50μm	1.5mm x1.5mm	1

V. CONCLUSIONS

An implementation of a method for the calculation of delay between two broad band digital signals has been presented. Results of digital simulations and tests executed on a FPGA showed that the method is functional and efficient, and exhibits an extended range that allows for measurement of delays up to $\pm 640 \mu\text{s}$ with a sampling speed of 200 kHz. Simulation results of this method using a standard CMOS 0.5 μm technology were also presented. Results of analog simulations showed a significant improvement of total power dissipation over other implementations. The efficiency of C²MOS dynamic techniques is thus corroborated, with new improvements being still possible by reducing supply voltage in the critical stages. Future steps include the realization of the integrated circuit and its verification.

VI. ACKNOWLEDGEMENTS

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